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GATE STRUCTURE WITH INDEPENDENTLY TAILORED VERTICAL DOPING PROFILE

Abstract

A gate structure for a semiconductor transistor is disclosed. In an exemplary embodiment, the gate structure includes a lower polysilicon region doped at a first dopant concentration and an upper polysilicon region doped at a second concentration, with the second concentration being different than the first concentration. A conductive barrier layer is disposed between the lower and the upper polysilicon regions, wherein the conductive barrier layer prevents diffusion of impurities between the lower and the upper polysilicon regions.